PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-048460
(43)Date of publication of application : 26.02.1993

(51)Int.Cl. H03M 1/46
H03M 1/08
H03M 1/12
H04N 1/40
H04N 1/40

(21)Application number : 03-236059 (71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(22)Date of filing : 17.09.1991 (72)Inventor : YAMAMOTO YASUNAGA
YAMAGUCHI KAZUFUMI
OKAMOTO TATSUSHIZU

(30)Priority
Priority number : 03133985 Priority date : 05.06.1991 Priority country : JP

(54) A/D CONVERTER AND SENSOR USING THE SAME AND THREE-DIMENSIONAL INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To apply the A/D converter to a 3-dimensional integrated circuit and an array sensor by devising the A/D converter in such a way that plural analog signals inputted in parallel are converted into digital signals at a high speed with high accuracy.
CONSTITUTION: This A/D converter is provided with plural analog signal input terminals 1an analog signal storage section 4plural comparators 10a single D/A converter 9a digital counter 5digital value storage sections 121415and a scanning circuit 16. The different analog signal fed to each analog signal input terminal 1 is stored in the analog quantity storage section 4 and inputted to a comparator 10 together with a reference output of the D/A converter 9 increasing gradually attended with the operation of the counterthe data of the counter when the reference output is higher than each inputted analog value is stored

individually to a digital quantity storage section 4 and the data therein is read sequentially as a digital value by the scanning circuit 16.

CLAIMS

[Claim(s)]

[Claim 1]Two or more analog value accumulating parts which accumulate each analog data inputted from two or more analog-data input terminal and two or more of these analog-data input terminalsA digital counter and a D/A converter which changes a digitized output of this digital counter into an analog valuecompared an output value and said analog data of this D/A converterand when said digital counter was a rise counteran output value of said D/A converter exceeded said analog data -- orTwo or more comparison means to distinguish that an output value of said D/A converter was less than said analog data when said digital counter is a down counterAn A/D converter provided with a digital value accumulating part which memorizes digital value of said D/A converter in response to control by two or more of these comparison means.

[Claim 2]An analog value accumulating part which accumulates each analog data inputted from two or more analog-data input terminal and two or more of these analog-data input terminalsA digital counter and a D/A converter which changes a digitized output of this digital counter into an analog valuecompared an output value and said analog data of this D/A converterand when said digital counter was a rise counteran output value of said D/A converter exceeded said analog data -- orTwo or more comparison means to distinguish that an output value of said D/A converter was less than said analog data when said digital counter is a down counterThe A/D converter according to claim 1 which is an A/D converter provided with a digital value accumulating part which memorizes digital value of said D/A converter in response to control by two or more of these comparison meansand was provided with a scanning circuit which reads an output of data of said digital value accumulating part one by one further.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]This invention relates to the sensor and three-

dimensional integrated circuit having the device which changes two or more analog values into digital valueand said inverter.
[0002]
[Description of the Prior Art]As a device (it is described as an A/D converter below) which changes an analog value into digital valuea found the integral typeAlthough various thingssuch as a successive approximation type and a flash plate typeexistall change one analog value into digital value serially in detail fundamentallyand do not change two or more analog values simultaneously. In the case of the image sensor which has an A/D converterthe gestalt connects to one analog output terminal common to each pixel of an image sensor the above A/D converters which have one input terminal fundamentallyThe analog signal value outputted serially is changed into digital value in detail.
[0003]
[Problem(s) to be Solved by the Invention]The following technical problems exist in the A/D converter of the above-mentioned conventional example. That isalthough the flash plate type A/D converter can carry out fast conversiona circuit complicates it by leaps and bounds with the rise of resolutionand a conversion rate is small [an A/D converter] although a found the integral type A/D converter is high degree of accuracy. By the three-dimensional integrated circuit which carries out signal processing of two or more analog value data organicallyand the sensor of the array form which obtains analog value data from two or more sensing elementsin order to perform various data processingit is necessary to carry out the A/D conversion of the data of an analog value generally inputted. Although an image sensor requires read-out of high-speed image data increasingly especially in recent years from a viewpoint of the improvement in manuscript reading speedand improvement in resolutionIt becomes difficult to carry out an A/D conversionwithout the influence of timea spike noiseetc. which the standup of an analog output waveform takes becoming large in connection with high speed readingtherefore reducing the accuracy of a signal value. It is necessary to change into digital value two or more analog values which distribute and exist in an inside inevitably in a three-dimensional integrated circuit at high speed. In this casealthough it is possible to change serial one by one serially at high speedcarrying out a multiplexer about two or more above-mentioned analog values using the A/D converter of large 1 input of circuit structure although it is a high speed of the number extremely smaller than the number of the analog value which should carry out A/D conversion processingIn this caseconcentration of many wiring to the large A/D converter of circuit

structure distributed in a three-dimensional integrated circuit from two or more analog values arisesand it is not desirable from a viewpoint of accumulation nature. It means that the wiring distance from an analog value output part to an A/D converter becomes longand the feature of a three-dimensional integrated circuit is not desirably harnessed from a viewpoint of S/N. The technical problem of ** which that only the number equivalent to the number of each analog value is provided with a flash plate type A/D converter does not have from a viewpoint of a degree of locationeither exists. Naturally the fixed pattern noise should be removed and the device for it is also required for the analog value by which an A/D conversion is carried out.

[0004]

[Means for Solving the Problem]In order to solve an aforementioned problem an A/D converter of this inventionAn analog value accumulating part which accumulates each analog data inputted from two or more analog-data input terminal and two or more of these analog-data input terminalsA digital counter and a D/A converter which changes a digitized output of this digital counter into an analog valuecompared an output value and analog data of this D/A converterand when a digital counter was a rise counteran output value of a D/A converter exceeded analog data -- orTwo or more comparison means to distinguish that an output value of a D/A converter was less than analog data when a digital counter is a down counterIt is the A/D converter provided with a digital value accumulating part which memorizes digital value of a D/A converter in response to control by two or more of these comparison meansand has a scanning circuit which reads an output of data of said digital value accumulating part one by one further. A sensor of this invention inputs an analog output of two or more sensing elements into two or more analog-data input terminals of an A/D converter of this invention. A three-dimensional integrated circuit of this invention inputs into each analog-data input terminal of an A/D converter of this invention each analog value distributed in a three-dimensional integrated circuit. In order to remove a fixed pattern noise of an analog value by which an A/D conversion is carried outa clamp circuit which consists of capacity and a switch for every analog-data input terminal of the above-mentioned A/D converter is provided.

[0005]

[Function]By the above-mentioned compositionthis invention. the analog signal from two or more analog-data input terminals -- each -- accumulating in the accumulating part which it has individually -- this -- each of an individual comparatorwhile transmitting to one input

terminal. The analog value which the D/A converter which follows on the increase in the digital value of a counterand increase or decrease in number gradually outputs is inputted into the input terminal of another side of said comparator in common as a reference value. When said reference value exceeds or is less than the analog value applied to one input terminal of said comparatorsaid each comparator output switches off to the timing based on the size of said analog signal value for every comparator. Said switch is connected to the digital value accumulating part which accumulates the digital value of said counter which it has for every pixel as an amount of binaries for every bit. Thereforewhen said switch is come by off based on the output of a comparatorthe digital value corresponding to the amount of analog signals for every analog-data input terminal is held at said digital value accumulating part. Conversion to digital value from the above analog value is performed in parallel about each analog-data input terminaland the time which this conversion takes is decided by count time of said counter based on predetermined analog upper limit. If the conversion to digital value from the above-mentioned analog value is completedthe data of the aforementioned digital value accumulating part will be outputted as digital value from a digitized output line one by one. By giving a lap by making the A/D conversion time and digital signal output time for every analog-data input terminal into timinglarge A/D conversion time can be taken with the increase in the number of analog input terminals. By having provided the clamp circuit for every analog-data input terminalBy clamping the end which passed capacity to the timing in which the voltage output which bears ****i.e.a light exposurehas appeared to the fixed voltage valueSince the voltage of the difference of an output appears [in the output terminal which passed the capacity of said clamp circuit to the timing in which an output appears at the time of dark] at the time of an output and dark at the time of above **a fixed pattern noise is removed.

[0006]

[Example]The example of this invention is described belowreferring to drawings. Drawing 1 is the 1st example of the A/D converter of this invention. In drawing 1it has two or more analog-data input terminals land these data is held at the analog value accumulating part 4 via the analog-data transfer switch 3 driven with the analog value transfer gate terminal 2. 5 is a counter and is controlled by the counter clock input terminal 6 and the counter clear terminal 7. 8 is a binary output line from the counter 5. In drawing 1since it is easythe counter 5 is used as three bit countersbut any bit counter may be actually used. D/A

converter 9 gives the data which changed the binary output from the binary output terminal 8 into the analog value to one input terminal of two or more comparators 10. The data held at said analog value accumulating part 4 is inputted into the input terminal of another side of each comparator 10. The data of the analog value accumulating part 4 is larger than the data of the analog output line of D/A converter 9 in a comparative initial stageThe output of the comparator 10 makes an ON state the 1st transfer switch 11 of digital dataand the data of the binary output line 8 is transmitted to the 1st accumulating part 12 of digital value as it is. If the counter 5 is a rise counterwhen the data value of the analog output line of D/A converter 9 will exceed the data of the analog value accumulating part 4the 1st transfer switch 11 of digital data changes to an OFF state for every analog parallel input dataThe data of the 1st accumulating part 12 of digital data continues holding binary data just before the 1st transfer switch 11 of digital data changes to an OFF state henceforth. After the counter 5 finishes count-up to the maximumthe data of all the 1st accumulating part 12 of digital data is held via the 2nd transfer switch 14 of digital data at the 2nd accumulating part 15 of digital value all at once with the digital value transfer gate terminal 13. The binary data held at the digital value accumulating part 15 of the following 2nd is read to the digital signal output line 18 one by one as digital value for every analog parallel input data via the digital data read-out switch 17 based on the parallel output of the scanning circuit 16. As for 19a scan start signal input terminal and 21 are scanning circuit carry pulse output terminals a scanning circuit clock input terminal and 20.

[0007]In parallel to the period to the digital signal output line 18 for every [by this scanning circuit] analog parallel input data when read-out is performed one by oneconversion to digital value from the analog value of the data of one group which made the sequence inputted into the next is performed in parallel for every analog input data as mentioned above. The analog value reset switch 22 is a switch for resetting the analog value accumulating part 4and is controlled by the reset gate terminal 23. This analog value reset switch 22 is required when the impedance of the analog-data input terminal 1 is largeand in particular when data input is performed to the analog-data input terminal 1 via a buffer with small output impedanceetc. it is not required. Although provided independently respectivelysince a counter full scale at the time of the analog parallel input data number which should be scannedand an A/D conversion generally differs between the scanning circuit clock terminal 19 and the scan start signal input terminal 20they are [this]

obvious. [of the counter clock input terminal 6 and the counter clear terminal 7] It is also possible to carry out the series connection of two or more A/D converters shown in drawing 1and to enable it to perform the A/D conversion of more analog parallel input dataThis is easily realizable if the scanning circuit carry output terminal 21 of the A/D converter of the preceding paragraph is received in the scan start signal input terminal 20 of the A/D converter of the next step one by one. Although the analog value accumulating part 4 and the digital value accumulating parts 12 and 15 are described as a capacitive elementthis is good also as a register which also contained the impedance conversion element further.

[0008]To the flip-flop used as an enable terminalespecially the digital value accumulating part 12 and the 1st transfer switch 11 of digital data the gate terminal of the 1st transfer switch 11 of digital data. The digital value accumulating part 15 and the 2nd transfer switch 14 of digital data are used as the flip-flop which uses the digital value transfer gate terminal 13 as an enable terminaland are good also as a static register. D/A converters 9 are common D/A converterssuch as a weighting type and R-2 R form. Although an A/D converter as shown in this figure enters under the category of the A/D converter called a found the integral type and a counter type and explained as a counted-up type in the above-mentioned explanationit is good also as a counted-down type. In a counted-down type casethe data of the analog value accumulating part 4 is smaller than the data of the analog output line of D/A converter 9 in a comparative initial stageAlthough the output of the comparator 10 makes an ON state the 1st transfer switch 11 of digital data and the data of the binary output line 8 is transmitted to the 1st accumulating part 12 of digital value as it isWhen the data value of the analog output line of D/A converter 9 is less than the data of the analog value accumulating part 4the 1st transfer switch 11 of digital data changes to an OFF state for every analog parallel input dataThe data of the 1st accumulating part 12 of digital data will continue holding binary data just before the 1st transfer switch 11 of digital data changes to an OFF state henceforth.

[0009]If the scan start signal input terminal 20 and the counter clear terminal 7 can be connected common and also a counter full scale and an analog parallel input data number are equal when considering it as an A/D converter only with one composition shown in drawing 1It is also possible to use themcarrying out common connection of the scanning circuit clock input terminal 19 and the counter clock input terminal 6. One example of the timing diagram for driving the A/D converter of

drawing 1 is shown in drawing 2. In drawing 2it is supposed that the scan output period of the digitized data is longer than an A/D conversion period. In order that an A/D conversion period and a digitized data output period may carry out synchronizationthe interval which can give analog parallel input data is decided by the period of the longer one of these both. In order for an A/D conversion period and a digitized data output period to carry out synchronizationH level period of the digital value transfer gate terminal must expire early rather than a digitized data output period begins. (The analog parallel input signal reset signal in drawing 2 is a thing in the case of resetting the data resources of the analog-data input terminal 1 of drawing 1and) It touches in explanation of the example of the sensor of below-mentioned this invention. Since the data which appears in the digital signal output line 18 in time is binary datahigh speed reading is possible for it one by one for every analog parallel input data. While this read-out is performedconversion to digital data from analog data is performed simultaneous in parallel in each analog parallel input data. An analog parallel input data number is 2500 temporarilyand if this is read from the digital signal output line 18 at 5 MHz with resolution of 8 bitsthe read-out period for 500 microseconds is needed. 1 clock period has been about 2 microseconds since the binary output line 8 and the digital signal output line 18 become eight and only 255 clocks should have been counted in said 500 microsecondsif the counter 5 was [the full scale] 255 in 8 bits. Thereforesince the operational amplifier of a low slew rate can be used as an inner device of D/A converter 9 so that the A/D conversion which is generous in time is [therefore] possiblethere is also no adverse effect of a glitch and highly-precise-izing is possible. Although it was considered as the A/D converter of the triplet by this example againit is in ** that it is easily extensible to the A/D converter of the arbitrary numbers of bits.

[0010]In drawing 2. Although the ** analog-data transfer switch 3the 1st transfer switch 11 of digital datathe 2nd transfer switch 14 of digital datathe digital data read-out switch 17and the reset switch 22 have given depiction and explanation as N-channel metal oxide semiconductor FET respectivelyNot N-channel metal oxide semiconductor FET but P channel MOS FETa parallel CMOS switchor JFET may be used. When taking into consideration further influence on the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switcha parallel CMOS switch is desirable.

[0011]Drawing 3 omits the digital value transfer gate terminal 13 and

the 2nd transfer switch 14 of digital data in drawing 1and is the 2nd example of the A/D converter of this invention. Since the thing of a number equal to the element used into drawing 1 with the element in drawing 3 is functionally equalit omits explanation. 24 in drawing 3 is a digital value accumulating part.

[0012]The timing diagram for the drive of drawing 3 becomes like drawing 4. That isa **** A/D conversion period appears in the inside of the interval to which an analog parallel input is givenand a digitized data output period appears succeedingly. That issince an A/D conversion period and a digitized data output period do not lap in timethe 2nd transfer switch of digital data is omissible. The composition of such an A/D converter has an effective full scale of the digitized output of an A/D converterwhen very small as compared with the amount of analog data by which a parallel input is carried out at once. For examplealthough the time which 5-MHz read-out takes 5000 to the number of parallel inputs is 1 m secondsthe A/D conversion period which set a full scale of the digitized output to 7and set the counter clock to 100 kHz will be about 70 microsecondsand is understood that this A/D converter is very small effective compared with 1 m seconds.

[0013]The series connection of the more than one is carried out like the A/D converter shown in drawing 1and the A/D converter shown in drawing 3 can also be enabled it to perform the A/D conversion of more analog parallel input data. Although the analog value accumulating part 4 and the digital value accumulating part 24 are described as a capacitive elementthis is good also as a register which also contained the impedance conversion element further. Especially the digital value accumulating part 24 and the digital data transfer switch 11 are used as the flip-flop which uses the gate terminal of the digital data transfer switch 11 as an enable terminaland are good also as a static register. This A/D converter is also good as counted-up type or countdown type any as well as the A/D converter shown in drawing 1. Since an A/D conversion period can use the operational amplifier of a low slew rate as an inner device of D/A converter 9 like the A/D converter of drawing 1 also in this A/D converter when small [enough] compared with a digital data output periodthe adverse effect of a glitch can be reduced. Although this example was also used as the A/D converter of a triplet againit is in ** that it is easily extensible to the A/D converter of the arbitrary numbers of bits. Although the analog-data transfer switch 3the digital data transfer switch 11the digital data read-out switch 17and the reset switch 22 have given depiction and explanation as N-channel metal oxide semiconductor FET respectively also in drawing 4Not N-channel metal

oxide semiconductor FET but P channel MOS FETa parallel CMOS switchor JFET may be used. When taking into consideration further influence on the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switcha parallel CMOS switch is desirable.

[0014]The 1st and 2nd examples of the sensor of this invention are shown in drawing 5 and drawing 6. Drawing 5 and drawing 6 add the sensing element 25 to each of the analog-data input terminal of the array form of the A/D converter respectively shown in drawing 1 and drawing 3. If each sensing element 25 accepts the portion and necessity which act as transformer Duce of the physical quantity which should be detected to voltage in drawing 5 and drawing 6the reset switch and buffer output circuit which initialize the primary detecting element itself are also included. (The operation timing figure of the reset switch described here is what was shown as an analog parallel input signal reset signal in drawing 2 and drawing 4and.) It is. For exampleif the signal in the primary detecting element in the sensing element 25 is an output form as currenteach sensing element 25 includes current/voltage conversion circuit. The sensor shown in drawing 5 leads the output of each sensing element 25 to the analog-data input terminal 1 of the A/D converter shown in drawing 1 in paralleland the following operations are as the timing diagram shown in drawing 2. The sensor shown in drawing 6 is also the samethe output of each sensing element 25 is led to the analog-data input terminal 1 of the A/D converter shown in drawing 3 in paralleland the following operations are as the timing diagram shown in drawing 4. It is possible to consider it as 1 chip integrated device or the hybrid integrated device which also includes an A/D converter by the sensor of such compositionand it can digitizewithout degradingthe accuracyi.e. S/Nof analog dataNot causing deterioration of a signal quality is mentioned as a feature by pulling out an output signal as digital data out of said device.

[0015]Although the one dimensional array-like sensor was explained in drawing 5 and drawing 6the sensor of two-dimensional array form is explained using drawing 7. 26 in drawing 7 is an area sensing element of an M line N sequenceand 25 The sensing element of a MxN individual27 is a vertical scanning circuit of M stageand 28 is a sensing element output terminal for every N sequencesThis sensing element output terminal 28 is connected to the analog-data input terminal 1 of the A/D converter respectively shown in drawing 1 or drawing 3and the scanning circuit 16 of an A/D converter is driven as a horizontal scanning circuitand a two-dimensional array form sensor is constituted. It drives so that the A/D

conversion and digital scan output of data of one line may be obtained for one step of every vertical transfer.

[0016]It is possible to consider it as 1 chip integrated device or the hybrid integrated device which also includes an A/D converter by the sensor of such compositionDeterioration of a signal quality is not caused that it can digitize without degradingthe accuracyi.e.S/Nof analog dataand by pulling out an output signal as digital data out of said device.

[0017]Drawing 8 shows the area sensor of the 1st more concrete example at the time of the sensor of drawing 7 being based on a CCD sensor. 31 is the A/D converter shown in drawing 1 or drawing 3. In drawing 8after the electric charge stored in each photo-diode 39 according to the incidence light exposure is transmitted to the vertical-charge-transfer way 41 by the drive of the transfer gate 40 for every vertical blanking periodthe vertical-charge-transfer way 41 is perpendicularly transmitted one by one by driving the clock pulse terminal 42. Henceforththe electric charge of each sequence is transmitted to the floating diffusion region 34 by the drive of the output gate 35 for every line for every horizontal blanking period. Said floating diffusion region 34 detects simultaneously the analog value which functions as a floating diffusion type amplifier and each electric charge in the floating diffusion region 34 has with the buffer 33and inputs this into the analog-data input terminal 1 of A/D converter 31 respectively. Belowfor every linethe A/D conversion of the analog data of each sequence is carried out in paralleland they are serially outputted to the digital signal output line 18 as digital value. It is for resetting by connecting the diffusion region 38 in which the reset gate 36 drives this and which is in reset potentialand said floating diffusion region 34 into drawing 8. 37 is a line for maintaining the potential of the diffusion region 38 at reset potential. 11819and 20 are respectively equal to the thing of the same number in drawing 1 or drawing 3.

[0018]Although explained as a sensor which has an A/D conversion function based on an interline transmission type charge transfer type image sensor in drawing 8the sensor which has an A/D conversion function similarly to the charge transfer type image sensor of a frame transmission type or a frame interline transmission type is realizable.

[0019]By the waysince this serves as a fixed pattern noise when the analog value given to two or more analog-data input terminals has a different offset value for every analog-data input terminalbefore carrying out the A/D conversion of thisit is necessary to remove. Thereforeif the clamp circuit which consists of capacitya switchetc. for

every analog-data input terminal is provideda fixed pattern noise is removable.

[0020]Thereforein the sensor of drawing 8it is good also as a thing including the correlated double sampling circuit which makes basic constitution the clamp circuit which consists the buffer 33 of capacity and a switch in order to reduce a noise. Namelyby clamping the output terminal of the clamp circuit of each sequence to fixed voltage immediately after keeping simultaneous the floating diffusion regions 34 of each sequence to reset potential about each horizontal blanking periodWhen the output which bear a light exposure all at once to the floating diffusion region 34 of each of said sequence appearsto the output terminal of the clamp circuit of each of said sequencethe output from which the fixed pattern noise was removed is obtained. In order to carry out an A/D conversion for every sequence by thisa suitable analog output is obtained.

[0021]Drawing 9 (a) shows the area sensor of the 2nd more concrete example at the time of the sensor of drawing 7 being based on an amplified type MOS sensor. The A/D converter which showed drawing 1 or drawing 3 31the element in which 47 forms a constant current sourceand 11819 and 20 carry out drawing 1 or the same number thing of drawing 3 respectivelyand they are that of a potato. In drawing 9 (a)all at onceand it is stored as gate potential of the transistor 45 for amplification. [the electric charge stored in each photo-diode 44 according to the incidence light exposure] [line / with selected work of a vertical scanning circuit] [for every horizontal blanking period] [the transfer switches 43] The transfer switch 43 is made into an OFF state after this. By making the drain of the transistor 45 for amplification high-level at this timethe follower output based on the gate potential of the transistor 45 for amplification of one line chosen now appears in the vertical output line 46 which is a common source of the transistor 45 for amplification. When the output of one certain line appears in the vertical output line 46the follower output which bears the light exposure information on the line first appearsThenthe follower output of the above-mentioned gate potential after the gate potential of the transistor 45 for amplification of the line was reset by the predetermined reset value with the transistor 49 for reset appears. By this sensorthe threshold voltage of the transistor 45 for amplification shows manufacturing characteristic dispersion for every pixeland this appears as follower output dispersioni.e.a fixed pattern noiseeven if the gate potential of the transistor for amplification is set as constant value. Thereforeit is required to take

the difference of the follower output which bears the above-mentioned light exposure informationand the follower output after reset. This method is explained below. When the follower output which bears the aforementioned light exposure information has appeared in the vertical output line 46the reset switch 48 which resets the potential of the terminal 51 by the side of the buffer 52 of the connection capacity 50 is made one. Nextafter the reset switch 48 of the potential of the terminal 51 turns offthe transistor 49 for gate potential reset of the transistor 45 for amplification is made oneand the follower output of the gate potential in reset potential appears shortly in the vertical output line 46. At this timethe voltage of the difference of the follower output of the gate potential in said reset potential and the follower output which bore said light exposure information appears in the terminal 51and this is respectively inputted into the analog-data input terminal 1 of A/D converter 31 for the output voltage of this difference for every sequence through the buffer 52. The fixed pattern noise resulting from characteristic dispersion of each transistor for amplification is removed by taking difference as mentioned above. The A/D conversion of the analog output of the difference of each sequence is carried out in parallel belowand it is serially outputted to the digital signal output line 18 as digital value. Hereafterif the analog output of the difference of each sequence of one line is inputted at a time into said A/D converter 31 in parallel for every horizontal blanking periodit is serially changed and outputted to digital value. An amplifier may be inserted between the vertical signal wire 46 and the terminal 51and when this amplifier consists of a voltage amplification part and a buffer stage which follows ita large output signal can be taken. Since the circuit which takes the aforementioned difference voltage is immediately after thisa fixed pattern noise is removed too.

[0022]Since the method for removing the fixed pattern noise used by the sensor of drawing 9 (a) works effectively also as a sensor which does not have an A/D conversion functionsuch a case is explained using drawing 9 (b). All at onceand it is stored as gate potential of the transistor 45 for amplification. [the electric charge stored in each photo-diode 44 according to the incidence light exposure] [line / with selected work of a vertical scanning circuit] [for every horizontal blanking period] [the transfer switches 43] The transfer switch 43 is made into an OFF state after this. Although the follower output which bears light exposure information at this time has appeared in the vertical output line 46the reset switch 48 which resets the potential of the terminal 51 of the connection capacity 50 here is made one.

Nextafter the reset switch 48 of the potential of the terminal 51 turns offthe transistor 49 for gate potential reset of the transistor 45 for amplification is made oneand the follower output of the gate potential in reset potential appears shortly in the vertical output line 46. At this timethe voltage of the difference of the follower output of the gate potential in said reset potential and the follower output which bore said light exposure information appears in the terminal 51. The amplifier 86 may be inserted between the vertical signal wire 46 and the connection capacity 50. When the amplifier 86 has a voltage amplification functiona large output signal can be takenand since the circuit which takes the difference voltage during an output also in this case at the time of an output and dark at the time of ** is provideda fixed pattern noise is removable too. A difference voltage value with an output is outputted to the common level output line 85 via the switch 84 one by one by the output pulse of a horizontal scanning circuit at the time of an output and dark at the time of ** which appeared in the terminal 51. Since the transfer switch 43 is turned off and the electric charge by exposure of this horizontal scanning period is separated from the gate of the transistor 45 for amplificationthe heterogeneity of the exposure time for every [that an output becomes large] sequence must have been producedso that it becomes a sequence read later.

[0023]According to the sensor of this inventioncan obtain above the suitable analog data for A/D conversion processing from which the fixed pattern noise was removedand digitization of the analog quantity of a sensing element at the place within the same chip as a sensor which approached. It makes it possible to carry out without a conversion time taking a long timeand data collection quality at very high speed becomes possible. Since this invention has a big effect also in hybrid compositionthe sensing element in which a raw material differs from the semiconductor used for the A/D converter can say that combination is possible and the scope is very wide.

[0024]This invention is applicable also in the sensing element treating other physical quantity which made not only light information but array formalthough the image sensor which treats light information as a sensor in explanation of the application to a sensor was taken up.

[0025]Nextthe example of the three-dimensional integrated circuit of this invention is describedreferring to drawings. Drawing 10 is a three-dimensional integrated circuit of the example of this invention. It consists of the 1st layerthe 2nd layerand the 3rd layer in drawing 10. The 1st layer is a photoelectric conversion layer and it consists of a five-line photoelectric conversion unit element child of five rows in

drawing 10. The 2nd layer is an A/D conversion layerand as shown in drawing 10it consists of a five-line A/D conversion unit element child of five rows corresponding to the optoelectric transducer of the 1st layer. The 3rd layer is a data-processing layer. What formed a signal transfer parta storage parts storea power supply sectionan actuatoretc. for every layer further as a three-dimensional integrated circuit existsand all generally have many the input or generating partsand A/D conversion parts of analog data used as a photoelectric conversion part in drawing 10. Although a layer [2nd] A/D conversion layer has the function to change many analog values into the digital value of a same number individualit doubles an A/D conversion unit element child part and an A/D conversion common partand shows drawing 11 the A/D conversion layer. In drawing 11the A/D conversion unit element child part is drawn as a form located in a line with two-line the array form of two rows. This A/D conversion layer is equivalent to what arranged what does not take into consideration the serial type of output of a digital value output in the A/D converter of drawing 1 which is the already described exampleand drawing 2 to two-dimensional matrix form. That isit is an A/D converter of the parallel input of two or more dataand the parallel output. It has two or more analog-data input terminals 61 which should receive analog quantity from the photoelectric conversion layer of drawing 10 in drawing 11and these data is held at the analog value accumulating part 64 via the analog-data transfer switch 63 driven with the analog value transfer gate terminal 62. 65 is a counter and is controlled by the counter clock input terminal 66 and the counter clear terminal 67. 68 is a binary output line from the counter 65. In drawing 10since it is easythe counter 65 is used as three bit countersbut according to the story tonality searched for theoreticallyany bit counter may be used. D/A converter 69 gives the data which changed the binary output from the binary output terminal 68 of the counter 65 into the analog value to one input terminal of two or more comparators 70 through the D/A converter analog output line 74. The data held at said analog value accumulating part 64 is inputted into the input terminal of another side of each comparator 70. The data of the analog value accumulating part 64 is larger than the data of the analog output line of D/A converter 69 in a comparative initial stageThe output of the comparator 70 makes the digital data transfer switch 71 an ON stateand the data of the binary output line 68 is transmitted to the digital value output terminal group 75 through the buffer amplifier 72. If the counter 65 is a rise counterwhen the value of the analog output line 74 of D/A converter 69 will exceed the data of the analog value

accumulating part 64Namelyto the timing which became independent for each photoelectric conversion unit element child of everythe digital data transfer switch 71 changes to an OFF state for every analog parallel input dataThe data of the digital value accumulating part 77 and the buffer amplifier 72 continues holding binary data just before the digital data transfer switch 71 changes to an OFF state henceforth. After the counter 65 finishes counting up to the maximumdo not carry out a graphic displaybut. If it has composition which samples the digital value output of each digital value output terminal group 75the digital value equivalent to the analog value given to each analog parallel data input terminal 61 will be obtained for every input terminal. The digital value obtained for every pixel below is transmitted to the data-processing layer of drawing 10and image processing is performed. The analog value reset switch 76 is a switch for resetting the analog value accumulating part 64and is controlled by the reset gate terminal 73. This analog value reset switch 76 is required when the impedance of the analog-data input terminal 61 is largeand in particular when data input is performed to the analog-data input terminal 61 via a buffer with small output impedanceetc. it is not required. Although the analog value accumulating part 64 and the digital value accumulating part 77 are described as a capacitive elementthis is good also as a register which also contained the impedance conversion element further.

[0026]Especially the digital value accumulating part 77 and the digital data transfer switch 71 are used as the flip-flop which uses the gate terminal of the digital data transfer switch 71 as an enable terminaland are good also as a static register. D/A converters 69 are common D/A converterssuch as a weighting type and R-2 R form. Although an A/D converter as shown in this figure enters under the category of the A/D converter called a found the integral type and a counter type and explained as a counted-up type in the above-mentioned explanationit is good also as a counted-down type. In a counted-down type casethe data of the analog value accumulating part 64 is smaller than the data of the analog output line 74 of D/A converter 69 in a comparative initial stageAlthough the output of the comparator 70 makes the digital data transfer switch 71 an ON state and the data of the binary output line 68 is transmitted to the digital value accumulating part 77 as it isWhen the data value of the analog output line 74 of D/A converter 69 is less than the data of the analog value accumulating part 64the digital data transfer switch 71 changes to an OFF state for every analog parallel input dataThe data of the digital value accumulating part 77 will continue holding binary data just before the digital data transfer

switch 71 changes to an OFF state henceforth. By the waythe data which appears in the digital value output terminal group 75 can be read all at once for every analog parallel input data. This is conditions desirable as an A/D converter of a three-dimensional integrated circuit. The A/D conversion element number per photoelectric conversion unit element child is smaller than a usual flash plate type A/D converter. A required component this as an A/D conversion unit element child about per photoelectric conversion unit element child A comparatorThe numbersuch as a digital data accumulating parta digital data transfer switchan analog-data accumulating partan analog-data transfer switcha reset switchand a buffer amplifieris also depended on consisting of a device of little [and] very easy structure. If the digitized output of this 11 figure is made into the triplet in order to illustrate simplybut the parallel number of the binary output line 68the digital data transfer switch 71and the buffer amplifier 72 is made into eightan 8-bit digitized output is easily realizable. Conversion to digital data from analog data is performed simultaneous in parallel in each analog parallel input data. What is necessary is to count only 255 clocks within a frame periodif a full scale of the counter 65 is 255For about 500 microsecondseven if it is a short frame periodit may drive with the clock of the comparison low frequency wave of a maximum of about 500 kHzThereforethe A/D conversion which is generous in time is possiblesince the operational amplifier of a low slew rate can be used as an inner device of D/A converter 69there is also no adverse effect of a glitch and highly-precise-izing is possible. Thereforealthough it is not so high-speed as a flash plate type A/D converterif it carries out from the frame frequency of the usual optoelectric transduceran A/D conversion high-speed enough and highly precise can be performedand a very highly efficient three-dimensional integrated circuit can be realized. Although it was considered as the A/D converter of the triplet by this example againit is in ** that it is easily extensible to the A/D converter of the arbitrary numbers of bits.

[0027]Although the analog-data transfer switch 63the digital data transfer switch 71and the reset switch 76 have given depiction and explanation as N-channel metal oxide semiconductor FET respectively in drawing 11Not N-channel metal oxide semiconductor FET but P channel MOS FETa parallel CMOS switchor JFET may be used. When taking into consideration further influence on the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switcha parallel CMOS switch is desirable.

[0028]What is necessary is just to give the potential of the terminal of

another side which bears light exposure information to the analog-data input terminal 61 in drawing 11when the voltage between the terminal changes according to a light exposure and should just fix terminal potential of one of these as a photoelectric conversion unit element child in the photoelectric conversion layer of drawing 10. For examplewhat is necessary is just to give the potential difference between the terminal to the analog-data input terminal 61 of drawing 11 using a photo-diode. A photoelectric conversion unit element child for drawing 12 to improve the charging capacity over the analog value accumulating part in drawing 11 is shown78 is a photoelectric conversion basic device represented by the photo-diode etc. It is connected by the gate terminal of the impedance conversion element 79 which takes follower circuitry for the terminal of one of these to carry out impedance conversion of another side at a fixed potential endand raise the current driving capacity as a photoelectric conversion unit element child. 80 is a reset switch for resetting the potential difference between both the terminals of the photoelectric conversion material 78. The pressure value which appears in the source terminal 81 of the impedance conversion element 79 is used for the analog-data input terminal 61 of drawing 11giving it.

[0029]As mentioned aboveaccording to the above compositionthe three-dimensional integrated circuit which is the degree of high integration in which it is possible to form a high-speed highly precise A/D converter for every unit optoelectric transducer with easy circuitry and a small element numberand high precision digital signal processing is possible is realizable.

[0030]Although the optoelectric transducer was made into the analog-data input sourcethis invention can be applied when the sensing device treating other physical quantity other than the light which made not only light information but array form is made into an analog-data input source. Even if the input source in particular of said analog data does not need to be an output from a sensing device and it is a certain analog value which appeared in process of signal processingintrinsicallyit is satisfactory and this invention is applied. If a clamp circuit is provided as drawing 9 (a) and (b) explainedif requiredit is possible to also realize the three-dimensional integrated circuit which has a removing function of a fixed pattern noise.

[0031]

[Effect of the Invention]As explained aboveaccording to this inventionby easy circuitrythe sensor which has a removing function of a fixed pattern noise becomes possibleand. If it becomes possible to save an A/D

conversion period to digital valueand to change into it two or more analog values by which a parallel input is carried out with high precisionthings and by carrying out rapid scanning of the changed digital valueand outputting itThe A/D converter of high-speed highly precise parallel input/serial output is realizable. By adding the sensing element of the array form which gives the analog data which should be inputted into the above-mentioned A/D converterIt can become possible to change the analog value based on various kinds of physical quantity amount of information of a sensing element into digital value in parallel for every sensing elementsaid digital quantity can be read at high speedand a high speed and the array form sensor of high S/N can be realized. For exampleif light is treated as said physical quantitythis invention is very useful as a picture input device. The above-mentioned A/D converter is considered as multi input multi-output compositionif the A/D conversion layer which carries out the A/D conversion of many analog values by this is formedit is highly precise and the three-dimensional integrated circuit which is the degree of high integration can be realized. In the object for three-dimensional integrated circuit division image processing for three-dimensional integrated circuits which has a sensing element of array formthis invention is especially very preferred.

[0032]As explained abovethe industrial effect of this invention is size very much.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]The circuit diagram in the 1st example of the A/D converter of this invention

[Drawing 2]The driving timing figure of the A/D converter of drawing 1

[Drawing 3]The circuit diagram in the 2nd example of the A/D converter of this invention

[Drawing 4]The driving timing figure of the A/D converter of drawing 3

[Drawing 5]The circuit diagram in the 1st example of the sensor of this invention

[Drawing 6]The circuit diagram in the 2nd example of the sensor of this invention

[Drawing 7]The lineblock diagram of the sensor of two-dimensional array form

[Drawing 8]The block diagram of the sensor of the two-dimensional array

form of the 1st example of this invention
[Drawing 9]As for (a)the block diagram (b) of the sensor of the two-dimensional array form of the 2nd example of this invention is a block diagram of the sensor of the two-dimensional array form which is not provided with an A/D conversion function.
[Drawing 10]The functional description figure of the three-dimensional integrated circuit of the example of this invention
[Drawing 11]The circuit diagram of the A/D converter used for the three-dimensional integrated circuit of this invention
[Drawing 12]A photoelectric conversion unit element child's circuit diagram
[Description of Notations]
1 Analog-data input terminal
4 Analog value accumulating part
5 Counter
9 D/A converter
10 Comparator
11 The 1st transfer switch of digital data
121524 digital-value accumulating part
13 Digital value transfer gate terminal
14 The 2nd transfer switch of digital data
16 Scanning circuit
25 Sensing element
31 Parallel yn- serial out A/D converter
34 Floating diffusion region
39 Photo-diode
40 Transfer gate
41 Vertical-charge-transfer way
44 Photo-diode
45 The transistor for amplification
46 Vertical signal wire
50 Connection capacity
51 Differential signal output terminal
61 Analog-data input terminal
63 Analog-data transfer switch
65 Counter
69 D/A converter
70 Comparator
71 Digital data transfer switch